UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/813,498	03/21/2001	Sharada Yeluri	004-5094	2092

22120 7590 03/11/2004

ZAGORIN O'BRIEN & GRAHAM, L.L.P.
7600B N. CAPITAL OF TEXAS HWY.
SUITE 350
AUSTIN, TX 78731

EXAMINER	
PAN, DANIEL H	

ART UNIT	PAPER NUMBER
2183	8

DATE MAILED: 03/11/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/813,498	Applicant(s) YELURI, SHARADA	
	Examiner pan	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 July 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 1-20 are presented for examination.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims1-5, 8,9, 11-14, 17,19,20 are rejected under 35 U.S.C. 102(e) as being anticipated by Lipasti (6,487,639).

3. As to claims1,3,8, 9,11, 12,17, 19,20, Lipasti disclosed a scoreboard system (e.g. see the memory tables in fig.3) comprising at least :

a) means for (or a module as in claim 9) for associating an instruction with index value (e.g. see the load data address which indicates the current data address accessed by load instruction in the indexed cache entry in col.6, lines 59-67, see also col.6, lines 5-9 for basic teaching of associating instruction with the index and the indexed entry in another table);

b) means (or module as in claim 9) for associating the instruction with the entry corresponding to the index (see the indexed entry by the load instruction in col.6, lines 59-67);

c) receiving an indication that a terminal event has occurred (see the negative result of the valid field in col.7, lines 5-19, see also the cache missed in col.7, lines 29-48);

d) means (or module) for invalidating the entry (e.g. see the negative result of the valid field for indicating no valid data in the entry in col.7, lines 1-19).

e) processor [10] (e.g. see fig.1);

f) a main memory (fig.1 [MAIN Storage}.

4. Lipasti did not explicitly characterize his tables as a scoreboard as claimed. However, no specific type of memory is being recited to describe the scoreboard in the claim. Therefore, the scoreboard is being treated as a label, or name to identify a given memory entity which has a plurality of entries with the indexed values. For example, scoreboard could be named " context table", or the like. Lipasti's table did have a plurality of entries and corresponding index for recording the information of the instructions (see col.6, lines 5-10, 65-66, see fig.3), and Lipasti's table also disclosed the functions, such as the invalidation etc, recited in the claim (see the paragraph # 3 above). Therefore, Lipasti's table did have the scoreboarding purpose. Applicant is welcome to provide feedback as to why the explicit word "scoreboard" should give a patentable weight compared to other memory entity which has the same usage but named differently.

5. Since no specific type of association being recited in the claim, the claimed language "associating" is interpreted as any information or operation being used related to the instruction. Lipasti's load data address was used to indicate the data address accessed by the load instruction. The load data address was an index to the corresponding load instruciton. Therefore, Lipasti's

load instruction and the data address being accessed by this instruction were associated. Applicant is welcome to provide feedback in the next reponse.

6. As to claims 2, 10, the indication of the valid field not equal to 1 indicating the subsequent status of the entry was an invalid entry .

7. AS to claims 4, 13, Lipasti also indicated the load data has been retrieved (e.g. see the outputting of the predicted value by the load instruction (e.g. see col.7, lines 17-19).

8. As to claims 5,14, Lipasti's index (the load data address) was also used to identify the entry (e.g. see the indexed entry in col.6, lines 65-67).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 6,7, 15,16 , 18, are rejected under 35 U.S.C. 103(a) as being unpatentable over Lipasti (6,487,639) in view of Ramagopal et al. (6,473,832) .

10. As to claim 6,7, 15,16, limitations of the parent clams have been discussed in paragraph #1, therefore, it will not repeated herein. Lipasti did not specifically show the forwarding (or receiving) the index value and the instruction to a load /store processing unit as claimed. Instead, it showed a general fetch and issue/decode units (e.g. fig.2). However, Ramagopal disclosed a load/store unit (e.g. see fig.1 [26]). It would have been obvious to one of ordinary skill in the art to use Ramagopal in Lipasti for forwarding (or receiving) the index value and the

instruction to the load/store unit as claimed because the use of Ramagopal could provide Lipasti the capability of the control circuit to adapt to particular access conditions of a given load or store instruction, thereby reducing the processing overheads of the main control circuit of Lipasti, and it could be readily achieved by configuring the read/write port of load/store unit of Ramagopal into Lipasti so that the load /store unit of Ramagopal could be recognized by Lipasti, and since forwarding the index value was already achieved by Lipasti using the load data address register 92 (see the register 92 for the purpose of forwarding the index value into a control unit in fig.3). Therefore, it should not be difficult to one of ordinary skill in the art to realize the forwarding (or receiving) of the index value into/from a dedicated processor, such as the load/store unit, was possible, for example, by providing a dedicated circuit bus for store and load instructions, and because Lipasti also taught that his instructions were passed to one or more execution units, each of the execution units had one or more pipelines that permit multiple instruction operated upon different stages (col.5, lines 41-50), which would have been recognized by one or ordinary skill in the art that the dependencies store and load instrcutions at different stages of processing usually were the factors causing the latency, and therefore providing a dedicated circuit control , such as a load/store unit, at a specific stage could have reduced the latency caused by the multi stage pipelines, and also expanded the processing capability of the control circuit of Lipasti, and in doing so, provided a motivation.

11. As to claim 18, Lipasti also included identified the entry (see the indexed entry in col.6, lines 65-67), and invalidating the entry (see the negative result of the valid field).

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Motomura et al. (5,305,458) is cited for the teaching of the load instruction associated with an index value (e.g. see the X2 instruction field in col.5, lines 15-25).

b) Burgess et al. (5,621,896) is cited for the teaching of index value with the corresponding valid entry for a store instruction (e.g. see fig.8).

c) Miyake (5,564,034) is cited for the basic teaching of the index address and tag address (e.g. see col.8, lines 40-61).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan Pan whose telephone number is 703 305 9696. The examiner can normally be reached on M-F from 8:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chan, can be reached on 703 305 9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DANIEL H. PAN
PRIMARY EXAMINER
GROUP